# Recording Autodialler

J. Shaw

*This is a digital recapture of the typewritten description of the autodialler produced in 1972.*

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# Recording Autodialler

The Autodialler was developed with the object of relieving the Subscriber of the task of dialling numbers repeatedly due to the called party being engaged. In particular dialling nine or ten digits several times then again hearing engaged tone is very frustrating and errors in dialling may be expected.

Design work was started in November 1971 and the first trials on the complete machine in April 1972. The designer was at this time completing the final year of a BSc. course. The present machine was made as a freelance "unofficial" project.

The Autodialler is capable of storing any number of up to ten digits previously dialled with the associated telephone and pulsing it out on demand. It can also store six numbers of up to four digits in a semi-permanent store. The store can be arranged as three numbers of up to eight digits.

The controls of the Autodialler are locked until the telephone handset is raised. Thus a number can only be autodialled if the telephone is used in the normal way. It is of course essential that dialling tone is heard before autodialling starts. The purpose of the above lock is to cause the user to supervise the call. An auto-recall facility is not provided.

Installation of the Autodialler is very straight forward involving a series connection to the line wires. With the power off, or with no control operated the Autodialler is seen as part of the line. Calls can therefore be made and received without operating the Autodialler. When the Autodialler is operated the handset is muted while pulsing is in progress, at the end of pulsing the line circuit reverts to normal. To clear the call the handset must be replaced, as usual.

List of Figures used in Text

# Recording Autodialler - User Instructions

## 1 Layout of Controls

The control buttons are not labelled but they may be identified by reference to fig. 1. The control buttons are mounted on coloured grounds. Each colour represents a different function.

The yellow ground has the executive controls; these will override any other control.

The blue ground has the semi-permanent store address buttons. Each button causes one number to be pulsed out and at the same time locks out all other 'blue' controls and the 'black' controls.

The black ground has the recording register controls. Each control locks out the other and the 'blue' controls.

Also mounted on the front panel are the mains on/off miniature toggle switch and a miniature indicator lamp.

## 2 Using the Autodialler

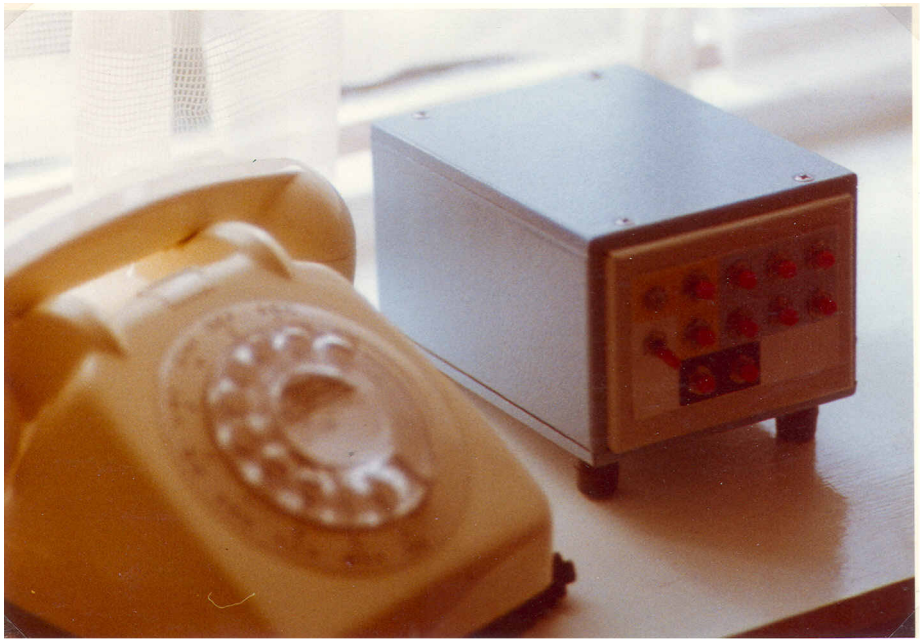
The mains switch must be pushed down, the indicator will not usually come on.

The telephone handset must then be picked up and dialling tone obtained; i.e. the procedure usually used to make a call (except dialling, though including any dialling needed to obtain an exchange line).

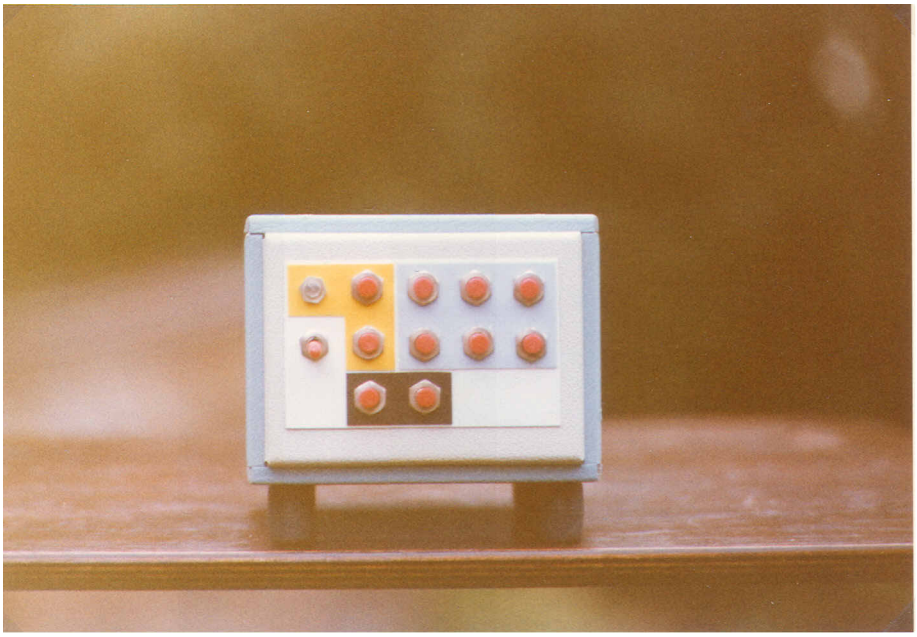
### 2.1 Recording a number

When it is likely that the call attempt will be unsuccessful due to the called number being engaged this procedure should be used.

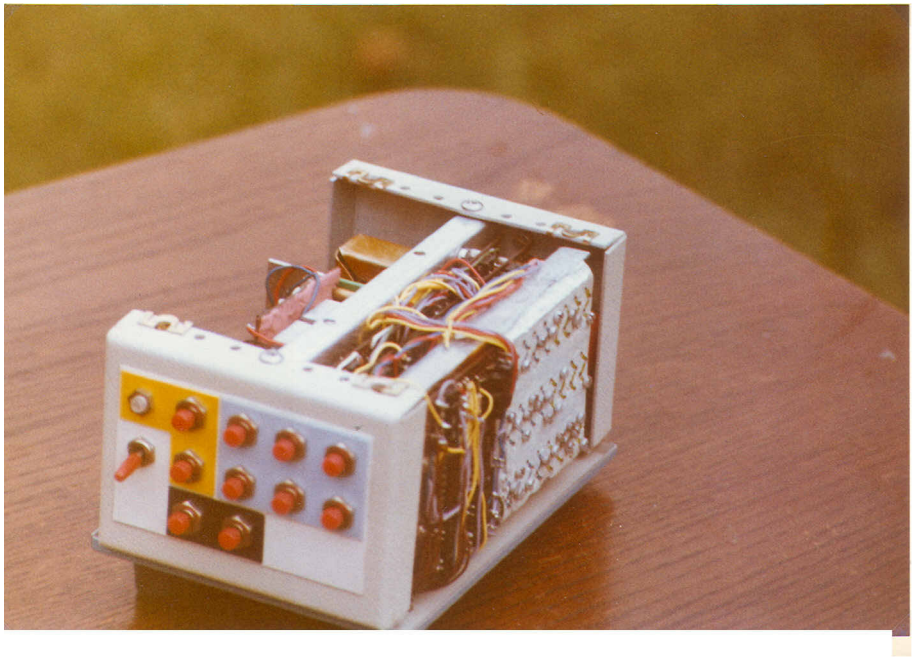
Before dialling ensure that the indicator is off. The RECORD control button should then be pushed. Using the telephone dial start dialling the required number. After the first digit has been dialled the indicator will come on. Continue dialling until the number is complete. If the call fails replace the handset and then regain dialling tone. When this has been done operate the PULSE-OUT REGISTER Button. The indicator will then flash as each digit is dialled.



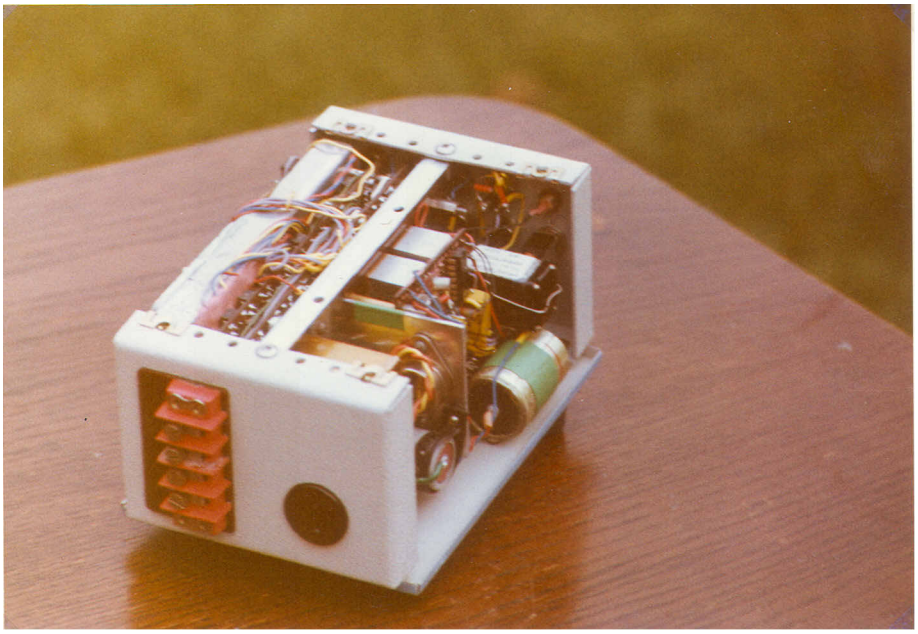
1 Typical Autodialler Installation



2 Autodialler Front Panel



3 Front Three-quarter View



4 Rear Three-quarter View

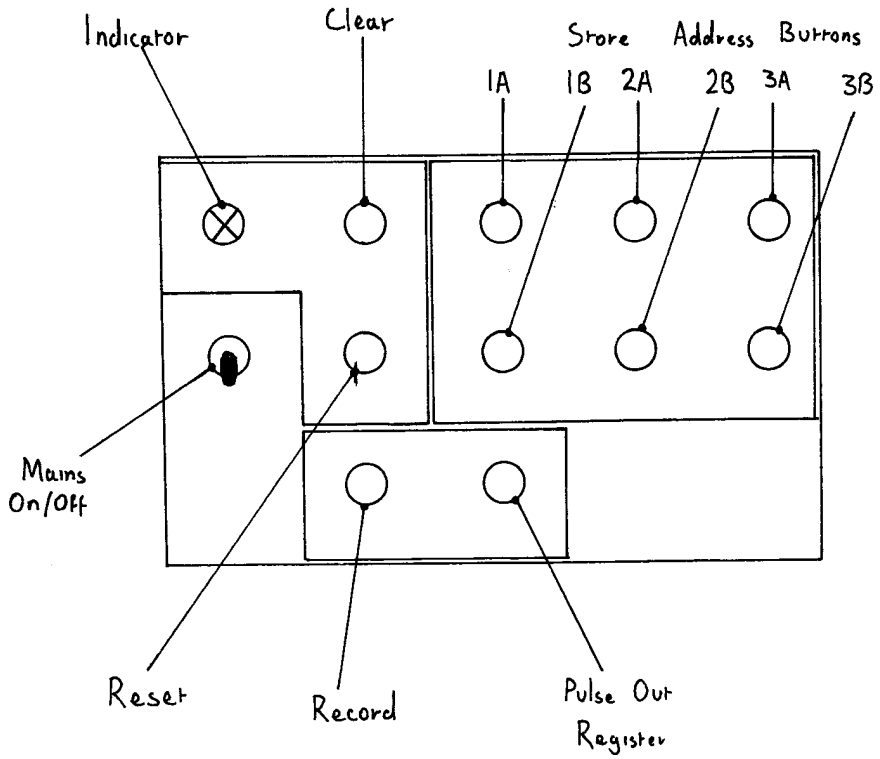



Fig. 1 Autodialler Control Panel

2.1 cont.

When the recorded number is no longer required the register may be cleared by operating the RESET and CLEAR buttons together. This will cause the indicator to go off. It should be noted that the record control is locked out if the indicator is on. Once the recording operation has started any digit dialled will be recorded; pauses may be made between digits (subject to limits imposed by the exchange, these also apply, of course, to any number dialled by the telephone alone.). Recording ceases when either the RESET control is operated or after the handset has been replaced for a short time. Best results will be obtained if Resetting is done after the last digit has been dialled.

It is important that power is supplied to the Autodialler whilst the indicator lamp is on (this indicates a number is in the register). If the power is switched off the number will be destroyed.

## 2.2 Autodialling a Stored Number

Each of the blue ground buttons when operated causes a number associated with it to be pulsed out. If the indicator is on it will flash as each digit is pulsed out, if not a different type of flashing will occur. It will be found that after pulsing out is complete the indicator will be in the same state as it was before autodialling started.

Each number is stored by means of several screws in an internal matrix (described later) because of this all stored numbers remain intact even though the power may be turned off. Because of the ease in autodialling these stored numbers they should be reserved for numbers often dialled or needed quickly in an emergency.

## 3 The RESET control

This is an executive control and will stop any operation in progress. It may be used during auto-dialling of the recorded number without fear of mutilating it; if the pulsing out control is operated the number will be autodialled correctly.

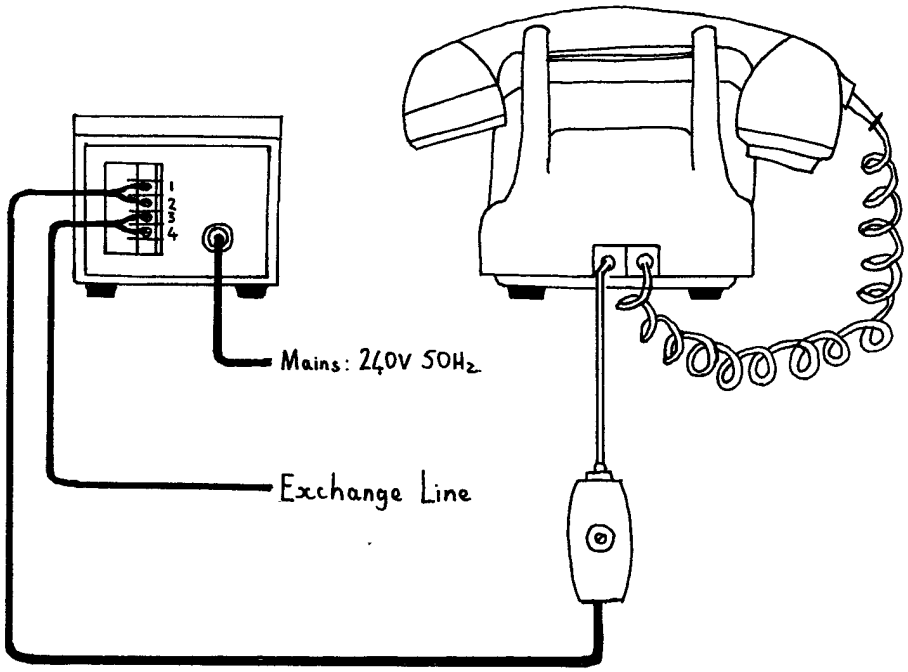



Fig. 2 Typical Autodialler Installation

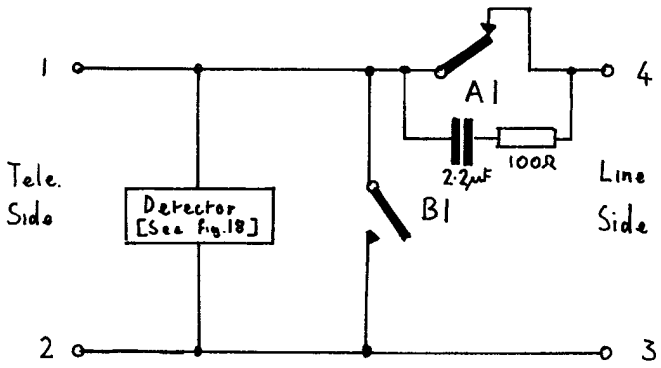



Fig. 3 Autodialler Line Circuit

## 4 Installation

As can be seen from fig. 2 and fig. 3 the Autodialler is a four-terminal device. It is inserted in series with both exchange lines; two of the terminals connect to the line, the other two to the line side of the telephone terminal block. It will be noted that two of the terminals are wired together internally; to obtain maximum muting of pulses heard in the handset it is important that they are wired to the line and telephone as shown.

A mains supply at 240 Volts 50Hz is also required; the power consumption is of the order of 5 Watts.

## 5 Storageof Semi-Permanent Numbers

On the right-hand side of the Autodialler, beneath the covers, is situated the screw matrix. It will be seen to consist of six areas, which are associated with the store address buttons as shown in Fig. 4. Each area is composed of four 'zig-zag' columns. Each column represents a digit. The value of each digit is determined by the position of screws in the four holes that make up a 'zig-zag'. The top hole has the value 1, the next the value 2, the next 4, and the bottom hole 8, as shown in fig. 5. The total value entered is equal to the digit. In all cases the first digit is the left-hand 'zig-zag' and the right-hand 'zig-zag' the last.

The screws used are 8 B.A. and need not be tightened to the same degree as one would normally use for mechanical purposes, excessive torque could damage the matrix.

This type of store was chosen from the point of view of cheapness and relative small size to demonstrate the principle of operation and is not put forward as a commercial design.

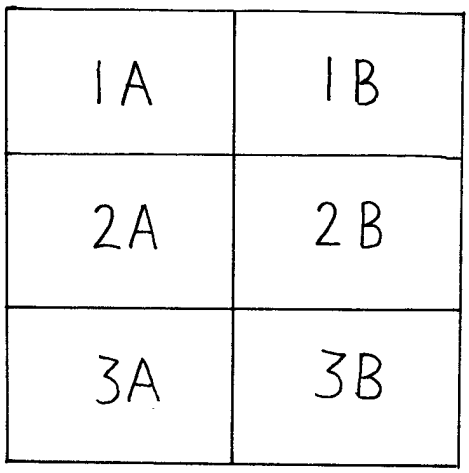



Fig. 4 Screw Matrix Organisation

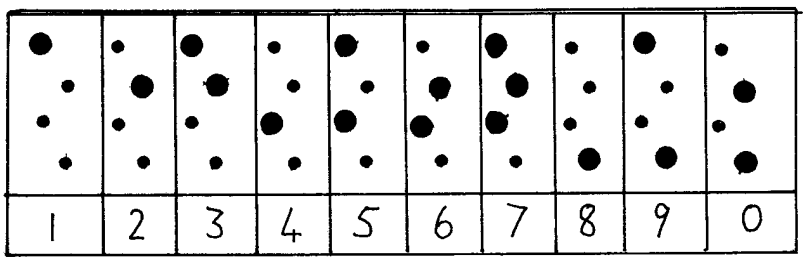



Fig. 5 Screw Positions for given Digits

# Recording Autodialler - Brief Description

## 1 Circuitry

The Autodialler uses Transistor-Transistor Logic (T.T.L.) extensively. The logic is mains powered via an internal power supply. Most operations are carried out synchronously; that is, operations take place at a time governed by an internal clock. This clock is in fact a multivibrator operating at about 1 kHz, giving a clock period of 1ms (one thousandth of a second). For reasons given later the frequency is slightly lower than 1kHz, but for most purposes the period can be regarded as being exactly 1ms.

The relays operating contacts shown in Fig. 3 are Mercury-wetted Reed types and are driven by transistors switched by the logic. Also shown in fig. 3 is the detector, this is either a moving coil relay or a plug-in transistorised replacement. This detector determines the state of the line, i.e. loop open or closed. It is used to lock the controls when the handset is on the rest and to repeat telephone dial pulses to the recording section of the Autodialler.

## 2 Operation of the line circuit

As can be seen from fig. 3 in the normal condition the Autodialler forms part of the line. When Autodialling starts contact B1 closes, looping the line with a low resistance path; contact A1 then opens and closes, operating as the pulsing contact. A capacitor and resistor across this contact act as a spark quench. The closure of contact B1 also mutes the receiver. To minimise the amplitude of the pulses heard it is important that loop currents due to dialling should flow through the minimum common path to handset currents, thus two connections are made to contact Bl and wired to separate terminals 2 and 3.

Because of the use of a master clock the pulsing relay is driven at a 2:1 on/off ratio. The on period is equal to 64 clock periods; the off period equals 32 periods

giving a total of 96 periods. As each period is nominally equal to 1ms this gives a total time of 96ms. The clock period is in fact slightly longer so as to give a dial speed of just under 10 p.p.s.. Thus all nominal times are in fact about seven percent longer than stated. A period of eight dial pulses is maintained between adjacent digit pulse trains, as each pulse is of approx. 103ms duration an Inter Digital Pause (I.D.P.) of 823ms is produced.

Dial pulses produced by the telephone are repeated by the detector and timed to eliminate spurious pulses due to contact bounce. This timing is dependent on the form of detector used. The logic can cope with the different sorts of detector used after very simple wiring changes have been made. Timing of the detector output is also used to determine the end of a digit pulse train during recording and to reset the Autodialler when the handset is replaced on the cradle.

Because of the form of logic circuitry used the Autodialler is able to accept a wider range of dial pulses and I.D.P.s than exchange signalling requirements call for, therefore there will be no problem of the Autodialler failing to record numbers from out of adjustment telephones, as it would be expected that dialled calls would fail to be switched by the exchange, hence drawing attention to the fault. Should the Autodialler timing fail its cause would be easily deduced.

# Recording Autodialler - Detailed Description

## 1 Autodialler Block Diagam

The Block Diagram in fig. 6 is an attempt at splitting the Autodialler into its component systems parts. As it was not part of the design objective to have separate easily identifiable sub-systems but rather to minimise the amount of hardware it would be difficult to identify these in practice. However as the Autodialler circuit is too complex to describe as a whole fig. 6 has been used as a basis for further description.

### Notes Applicable to all the following Circuit Diagrams

In the diagrams that follow it will be seen that a circle is used to indicate a gate; a plain circle indicates a NAND gate as in the logic family used this is by far the most common. Different types of gate are shown by markings inside the circle, e.g. a '1' with a bar above designates a NOR gate, an X an Exclusive OR gate. These symbols are somewhat unconventional but as the British Standard appears to change from year to year, and as they are easy to draw but above all, because they assisted the design of a working machine they have been used here.

The notes with the diagram assume that the reader is familiar with the action of the above types of gate, but even if not some insight into the working of the Autodialler should be gained.

It may appear that the numbers given to the various gates are not in any sort of order; this is because they are partially allocated on the basis of the gate's physical position and are used on the design diagrams. It would have led to confusion if the numbers had been changed here.

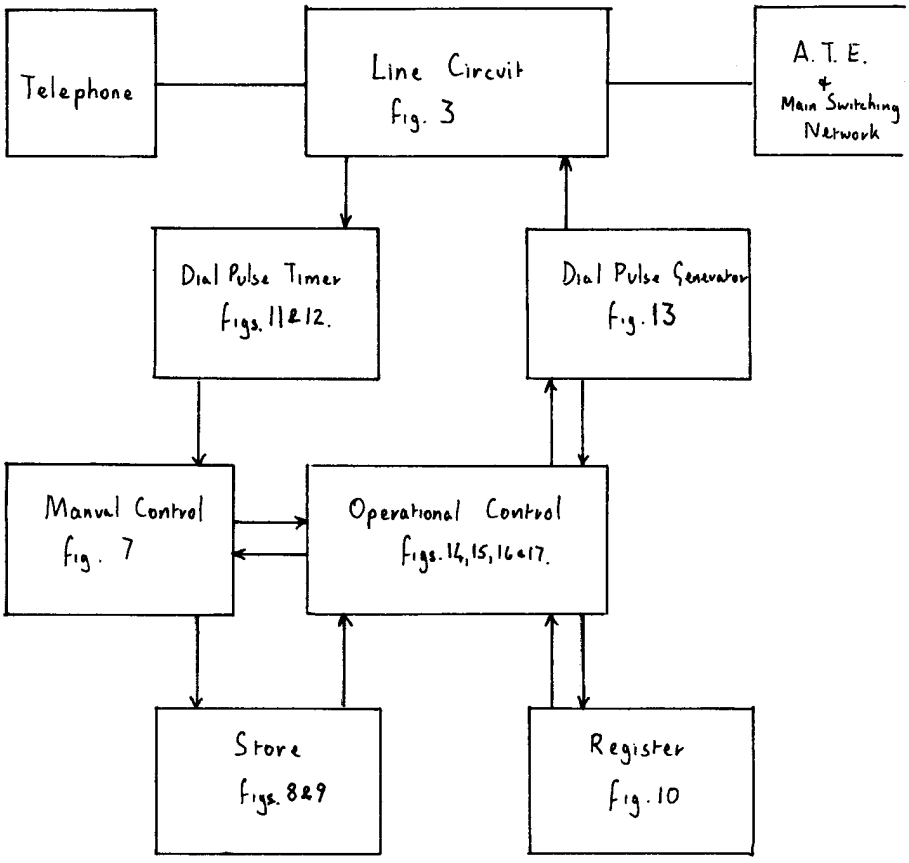



Fig. 6 Autodialler Block Diagram

## 2 Manual Controls

The ten push-buttons on the front panel cannot be connected directly to the operating logic circuits as it is important that control pulses are of an exact duration and occur in synchronisation with other machine originated pulses. The circuit depicted in fig. 7 performs this function.

With the RESET button in the normal position the effect of gates 65, 20,and 68 is to apply a '0' to the bus feeding the store address buttons and the register pulse-out button. Because of the 1ms clock input to gate 20 this '0' is synchronised with clock controlled functions. It will be noted that if the RESET button is depressed the bus will be continuously at '1'. The same condition will result if the handset is on the cradle as control (0) will be '0'. The open-circuit inputs of the Data Latch (D1 to D8) are seen as 'l's. If the handset is raised and one of the address buttons operated the associated D input will become '0' and the corresponding output, LQ, also becomes '0'. All other LQ s are still '1'. The output of gate 64 then changes state to '1'. When this occurs all the inputs to gate 50 are 'l', the output is then '0'. This output is the control lock and is connected to the 'clock' input of the Data Latch. It is a property of the latch that if the 'clock' is '0' all D inputs are shut out and the outputs retain the previous state. Thus should any other address button be pushed it will not be effective.

When the operation has been carried out one of the inputs to gate 50 will become '0', this releases the lock as the state of the now released address button can now be entered into the latch.

The control lock also operates on the RECORD control with the addition of a further lock provided by the state of J-K 6; the result of this is that RECORD cannot be selected if there is already a number in the register. This control is effected via gate 66.

It will be realised that when a number is to be pulsed out from store that the operation is identical to pulsing out any other number from store, with the exception of the

actual digits pulsed out. A control signal designated Pw is therefore produced. As described earlier the output of gate 64 changes when one of the address buttons is pushed, but this is true if RECORD or P.O. REGISTER is operated not just when a store address button is operated. Therefore gate 56 is used to distinguish between a change in the output of 64 due to a Pw operation or the other two. If the change is due to a store pulse out instruction LQ 1&2 will be '1', as will 64 output, therefore 56 output will be '0'. If, say, RECORD had been operated LQ 1 would be '0' and 56 output would become '1'. Thus 56 output is equivalent to $\overline{Pw}$ .

Should the user desire to stop an operation in progress the RESET control must be used. As explained earlier operating this control causes the bus to become '1'. This has no immediate effect but the control forces gate 50 output to the 'if state, opening the D inputs. If all the buttons were at normal the circuit would reset, it is possible though that a button may be held down, but as the bus has changed state all D inputs are '1' even if some are depressed.

To empty the register CLEAR must be operated. As a safeguard RESET must also be held down. An output $\overline{CR}$ is produced, this resets J-K 6 (mentioned in conjunction with the RECORD lock) and splits the register in several parts. A stream of pulses at clock frequency are produced at the output of gate 67 when CLEAR is operated. These cause the data in the register to shift but as CR sections the register the data will be destroyed within 8ms.

Also produced by this circuit are the control signals R (Record), Pr (Pulse out register) and the store addresses lA, lB, etc. The Data Latch also has complemented outputs so all these signals are available in true and complemented forms. It should be noted that as the manual command signals are effectively inverted the true form of the control signal must be taken from $\overline{LQ_n}$ i.e. $LQ_1=\overline{R}$ .

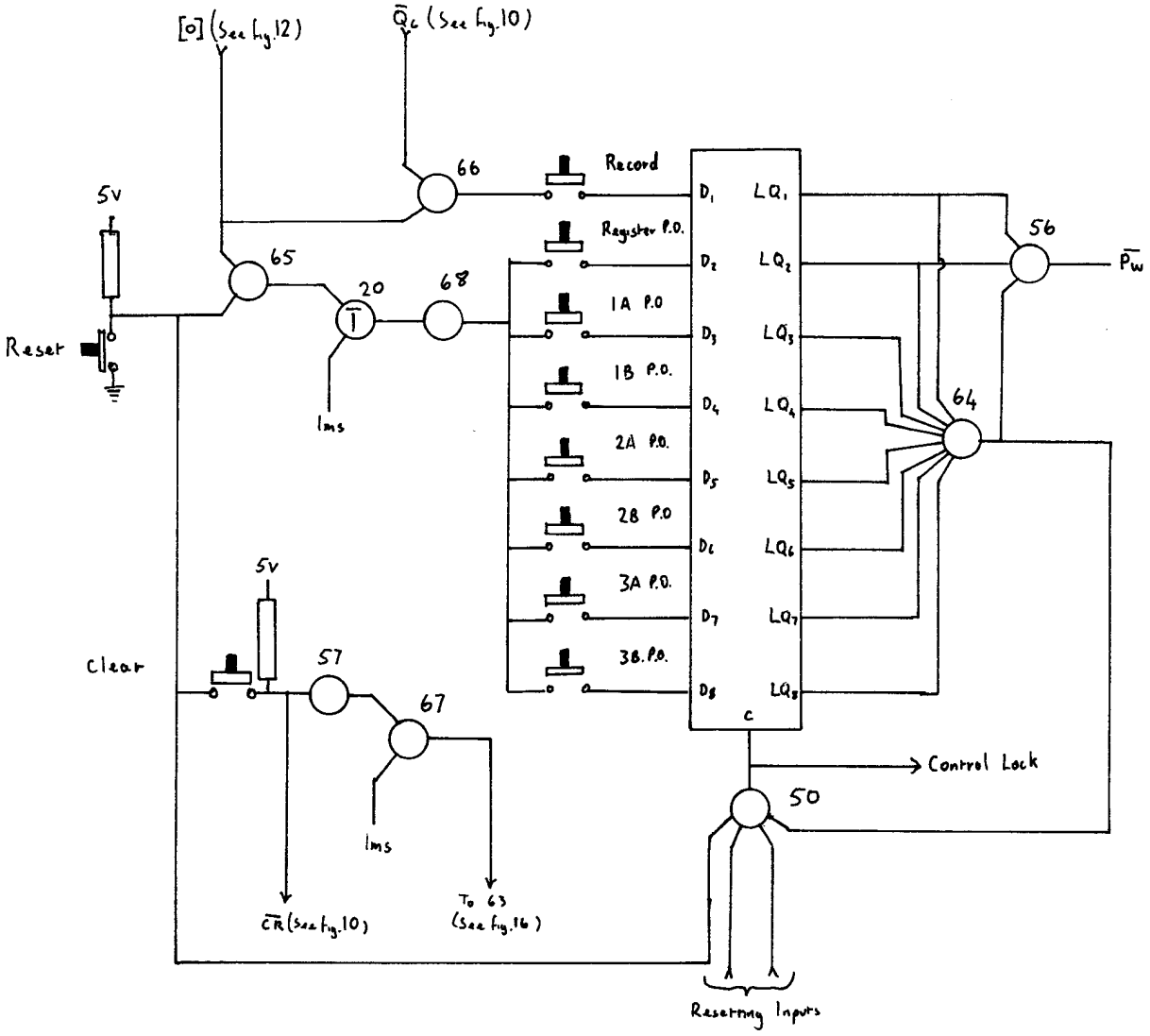



Fig. 7 Manual Controls

## 3 The Semi-permanent Store

The store is taken to mean the store address circuit, the store itself and the data selectors. Thus as a sub-system the store has an address line for each sub-store, a master address line ( $\overline{Pw}$ ) three digit selection lines and four data output lines.

The store itself consists of 96 8 B.A. nuts in 6 groups of 16. When $LQ_{3-8}$ are '0' the 16 nuts that form a sub-store are at a voltage near to the logic supply rail. Behind each nut and insulated from it is another nut to which is soldered a diode. Thus when a screw is in the matrix it connects the two nuts together. In this way the input of a data selector connected to a diode at 'high' voltage is held at the '1' state. If there is no screw, or the sub-store isn't energised the 470 ohm resistor at the selector input holds that input at '0'. The diodes of course prevent voltages at one input from being 'seen' at the inputs of other selectors. This circuit is illustrated in fig. 8; it should be noted that there are a total of six transistors, driving 96 diodes, which concentrate onto 32 selector inputs, each selector having 8 inputs.

The selection circuit is shown in fig. 9. When the control line $\overline{Pw}$ is at '1' the selector output is held at '0'. With $\overline{Pw}$ at '0' i.e. Store addressed, the selector output Y takes the state of the data input selected by the selection lines. These lines operate in natural binary, thus with all selection lines at '0' the data at input $D_O$ is seen at Y. The output of each selector is weighted thus $S_A$=1, $S_B$=2, $S_C$=4, $S_D$=8. Taking all the outputs together it is possible to represent a decimal number.

Taking both circuits together; 1) The sub-store is selected, Pw ='1'. 2) Certain inputs of all the selectors become '1' depending on the position of the screws. 3) The selection lines cause the selector to look at inputs $D_{OA}$, $D_{OB}$, $D_{OC}$, and $D_{OD}$. A coded decimal number is seen at the output. 4) Under the control of the Operational Control Section the selector is subsequently 'driven' to scan the remaining inputs until all the relevant numbers have been pulsed out. 5) Control is then reset.

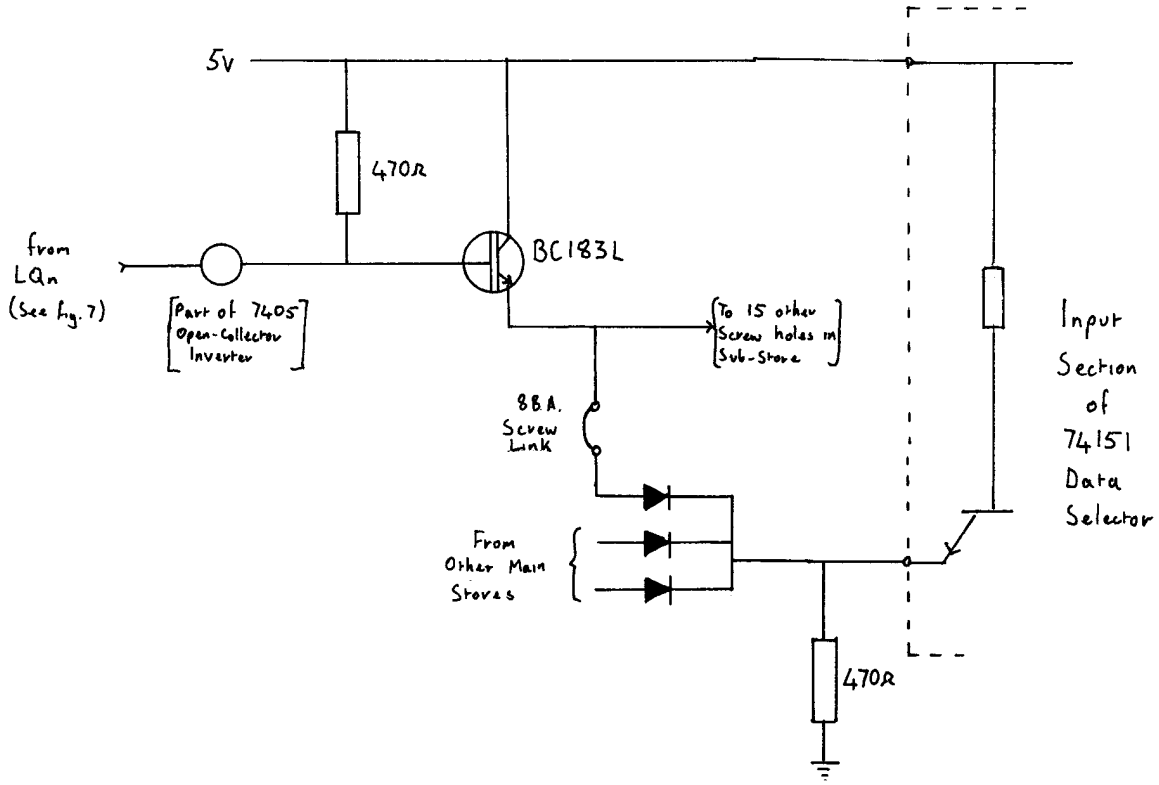



Fig. 8 Store Address Circuit

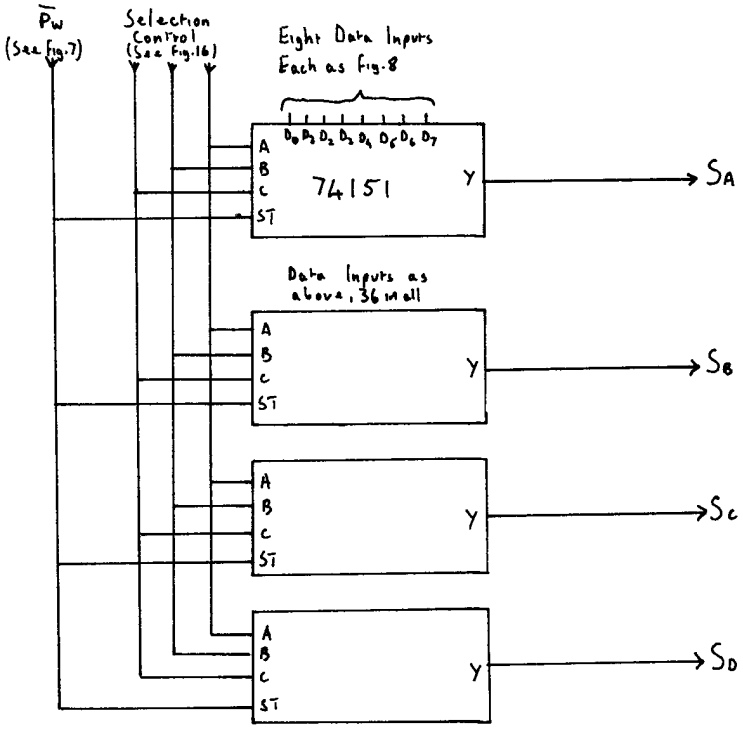



Fig. 9 Store Data Selector Circuit

## 4 The Register

The register is used for the short-term storage of a telephone number dialled by the user. The register takes the form of one 5-bit shift register and five 8-bit shift registers. The effective capacity is 40 bits, allowing the storage of 10 digits, (10 x 4 bits). The register could be extended if more storage was required.

As can be seen from fig. 10 the 5-bit register is more complex than the 8-bit registers; it is provided with outputs and pre-setting inputs for each bit, whereas the 8-bit registers have serial input and output facilities only.

When a number is being recorded the 5-bit register is cleared and the number presented at inputs $C_A$, $C_B$, $C_C$, and $C_D$ is entered by operating the preset. The inputs are then locked out when the preset is normalised. Four shift pulses are then applied to CP; this has the effect of shifting the data entered into the first four bits of the first 8-bit register. It will be noted that the input to the right-hand bit of the 5-bit register is earthed, thus no data can be entered. When shifting starts each bit of the first digit is shifted in sequence through this empty part of the register (it is also shifted in parallel to the first bit of the 8-bit register). As a number has been entered the output of this stage must be '1' at some time during the shift. J-K 6 will then be set and the indicator comes on via gate 36 and the transistor driver. Because J-K 6 is set the record mode cannot be selected again until the register is cleared. When this is done CR is '1' and the bistable is reset.

The input DP to 36 is the output from the internal dial pulse generator. When a dial pulse is present the indicator will either come on or go off depending on its previous state. The indicator therefore shows that pulsing out is in progress by flashing regardless of whether there is a number in store or not. At the end of pulsing the indication is steady and the same as before pulsing started.

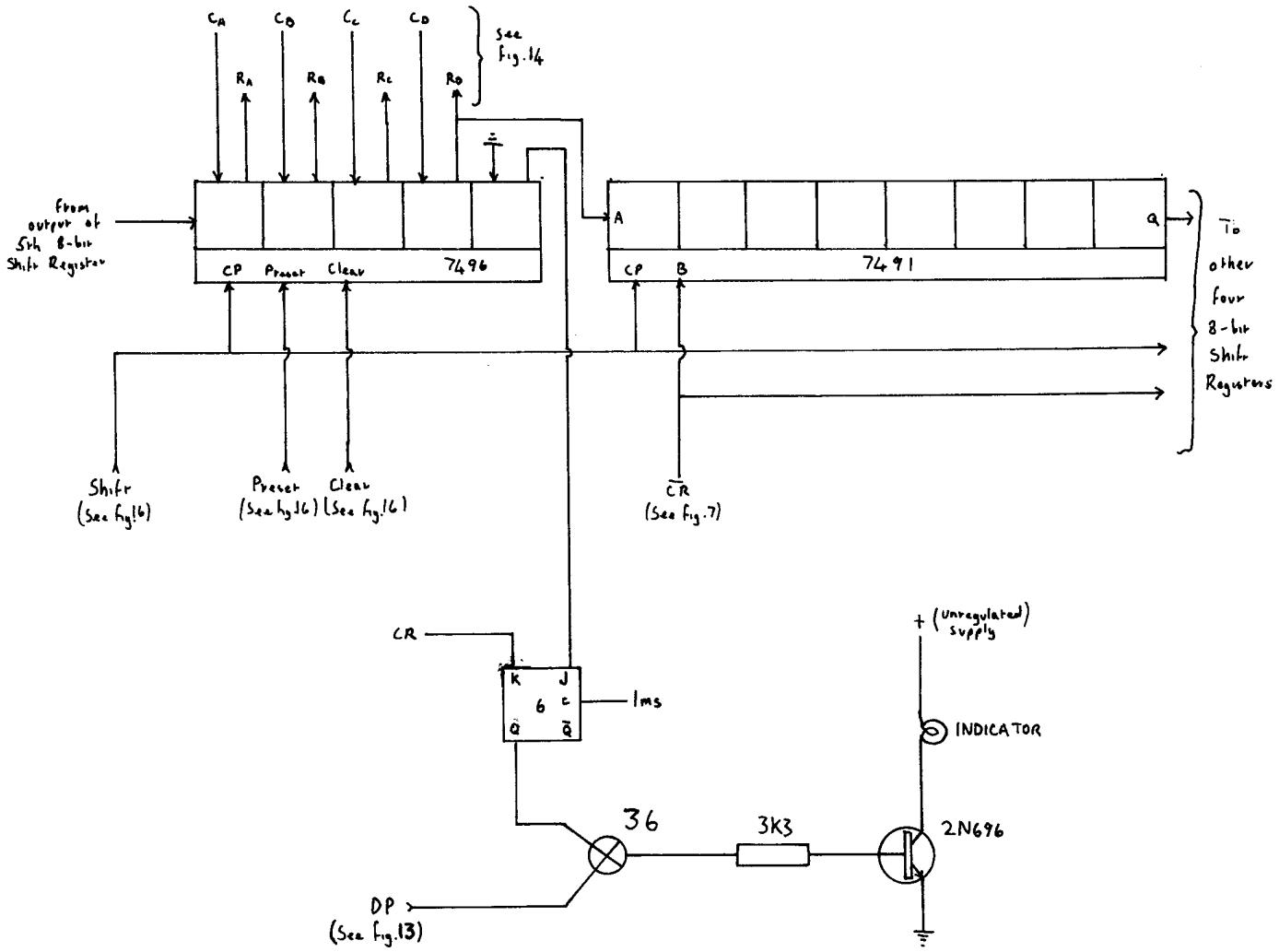



Fig. 10 Register and Indicator Circuit

## 5 Dial Pulse Timing

In order that a number can be recorded it must be possible to convert the signals sent from the telephone to the exchange into a form that can be manipulated by the Autodialler. This operation is carried out by the detector. The detector output is high if the telephone line is looped and low if not. As the pulse that the telephone dial produces represents part of a number it was designated [1] (= break) and because the detector output is low in this case inversion is provided by inverter 1. The output of 1 cannot be used directly as contact bounce will cause an error at the detector output. The pulses therefore have to be timed. The time reference is provided by the Autodialler 'clock'. As stated earlier this operates with a period of approximately 1ms, but the duration of a dial pulse is of the order of 66ms.

Fig. 11 shows the counters that provide timing signals for the Autodialler. Each stage of each counter divides by two; that is to say the period at the output is twice that of the input period. Above each stage is marked the output period. It must be noted that the output will be low for half the period and high for the other half. When timing is in progress gates 39 and 42 have no effect and need not be considered here.

Fig. 12 shows the circuit used for discriminating between 'breaks' and 'makes'. With the handset off the rest the input to D-type 1 is '0', the output Q will also be '0'. If a number is dialled the loop will be broken as the dial returns; the input D will therefore be '1'. The value of the input will only be transferred to the output Q on the rising edge of the 1ms clock pulse. During this period the input and output $\overline{Q}$ are the same and the output of gate 2 changes to '0'. This has the effect of resetting and stopping the timing chain in fig. 11. Within 1ms the input at D will have been passed through to output Q, the timing chain is now started. Inputs $t_1$ and $t_0$ are derived from this chain, using the transistor detector $t_1$ will rise after 16ms gate 4 output will fall and gate 3 output will rise.

This output is connected to the clock input of D-type 2 and because it has just risen the output $DQ_1$ is transferred to output $DQ_2$. It will be realised that if the detector output changes during this period timing is restarted. Thus spurious input pulses are discounted. Timing for 'makes' is similar. Timing continues until after 256ms have elapsed when the state of D 2 is 'memorised' by either the bistable formed by gates 8 and 10 or gates 9 and 11. These produce controls [1] and [0]. When these are high it indicates either that the loop has been open for greater than 256ms (handset replaced) or that the loop has been closed for greater than 256ms (Inter Digital Pause).

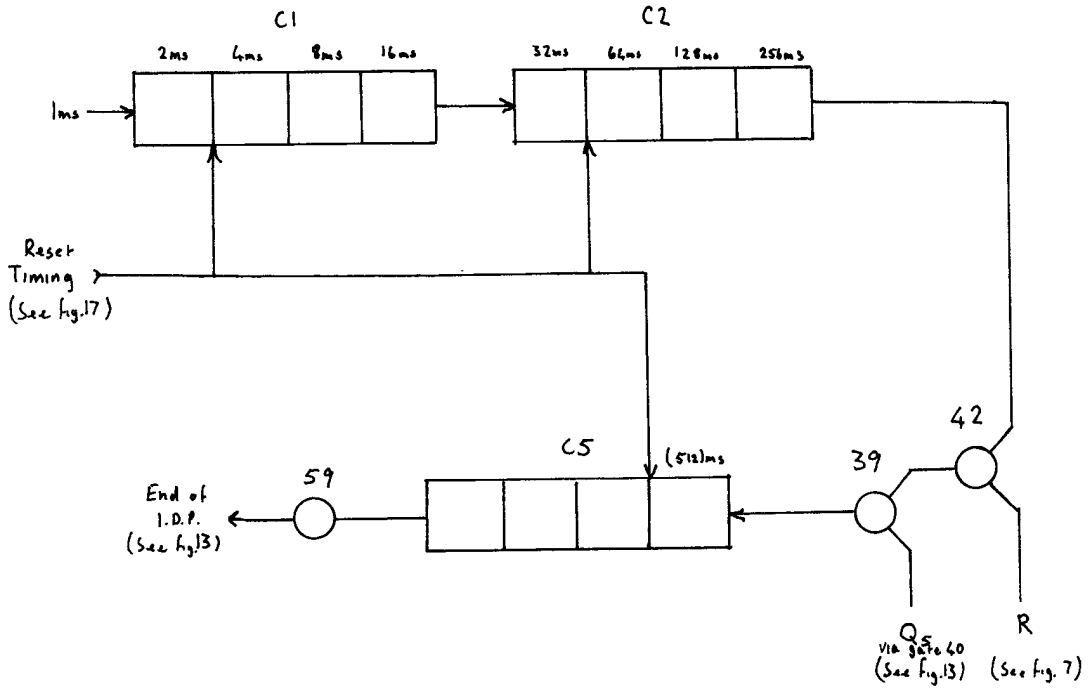
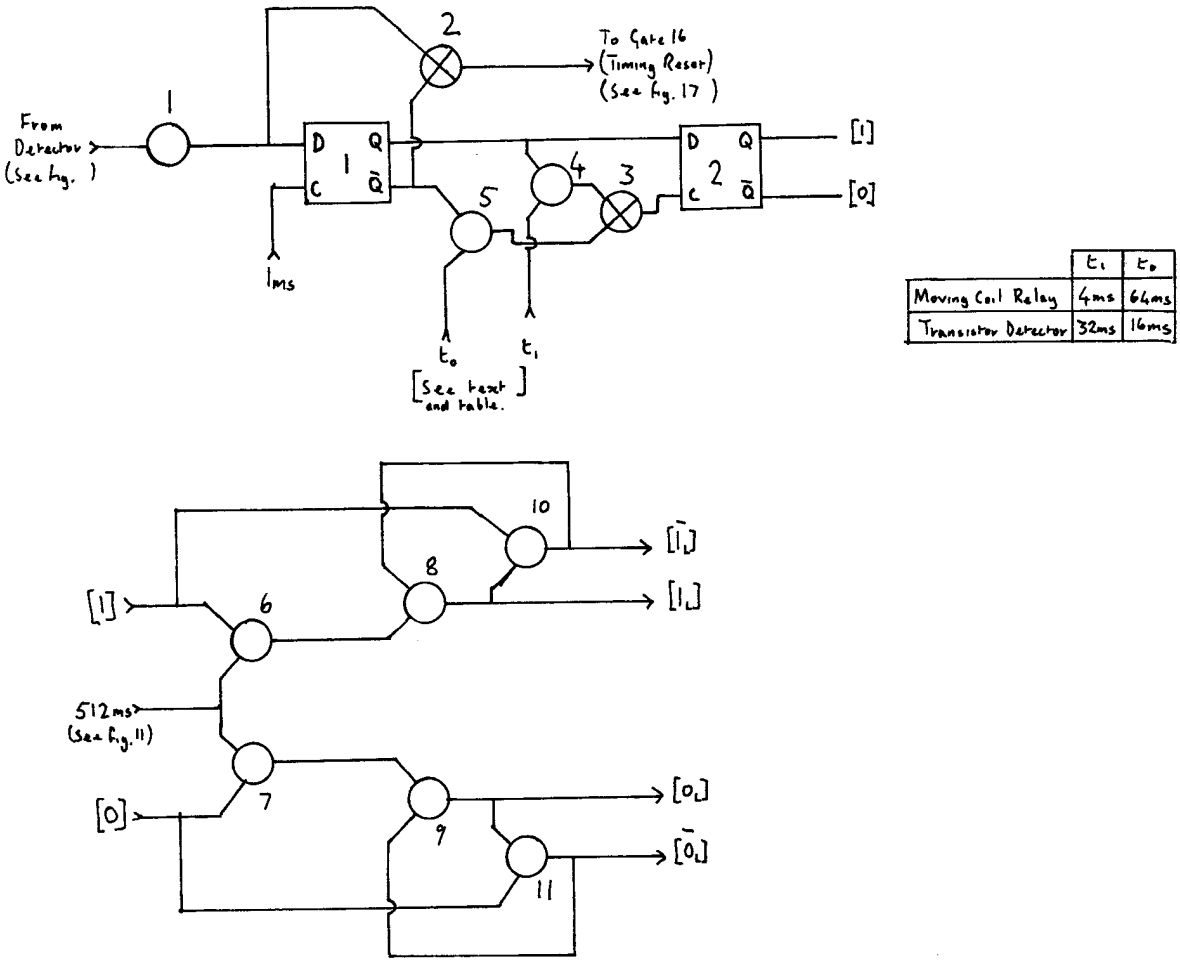



Fig. 11 Timing Circuit




| | $t_1$ | $t_0$ |
|---|---|---|
| Moving Coil Relay | 4ms | 64ms |
| Transistor Detector | 32ms | 16ms |

Fig. 12 Dial Pulse Discrimination

## 6 Dial Pulse Generation

The Autodialler must, by definition be capable of producing dial pulses. The circuit that carries out this function is shown in fig. 13.

The actual line switching is carried out by relay A and therefore the purpose of this circuit is to provide an operating signal for this relay. Because the relay can operate within a few milliseconds operating lag is ignored, (in any case the release lag is similar so the two will tend to cancel). For 10 p.p.s dialling the relay should be on for 66.6ms and off for 33.3ms during pulsing.

The J-K flip-flops 4 and 5 are coupled together in such a way that $Q_5$ is high for two clock periods and low for one. The clock in this case is the 32ms output from the timing chain (see fig. 11); the output is therefore high for 64ms and low for 32ms. As mentioned in the Brief Description these times are slightly longer, but the 2:1 ratio is preserved. The $\overline{Q}$ output was used because the clear facility provided on this type of flip-flop causes $\overline{Q}$ to be high when operated, by making use of this the generator can always be started with the output high.

The J-K flip-flops 2 and 3 are used to control dialling, both are normally reset. When dialling is to start both 2 and 3 are set. $Q_2$ goes high having been low" which caused 4 and 5 to be held reset, this releases 4 and 5 which act together as the generator. As $Q_3$ is high dial pulses DP are available at the output of gate 35. When the autodialled number equals that to be sent the Parity line goes high and hence $\overline{P}$ goes low (see fig. 14) this resets 3 and pulsing out ceases. The generator however continues to run, pulses at dial frequency appearing at the output of gate 40. These pulses are counted by C5 (fig. 11), when eight pulses have been counted the output of gate 59 falls and this resets J-K 2; the dial pulse generator is now stopped and preset ready for the next digit to be sent. It will be seen from fig. 11 that C5 is disconnected from the timing chain by the action of gate 42. The period between J-K 3 being reset and J-K 2 also being reset is the I.D.P. which is in this case equal to eight dial pulse periods (aprox. 823ms).

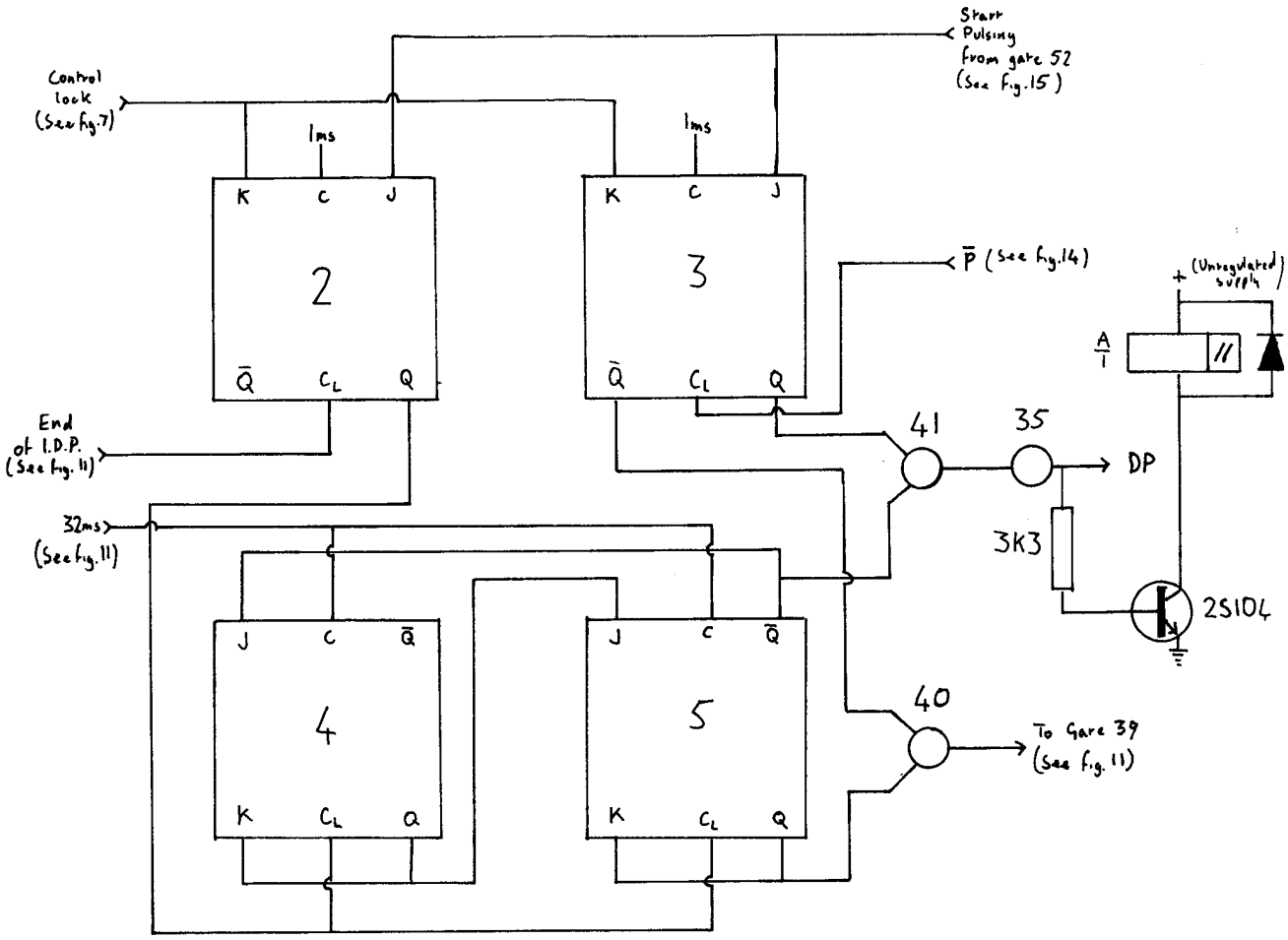



Fig. 13 Dial Pulse Generator

## 7 Operational Control

This category includes those parts of the circuit not yet described. These circuits control the operations needed to call numbers from store, send the dial pulses corresponding to these numbers and then return control to the user.

The data from the store and register is presented to the control section and compared by means of the circuit shown in fig. 14 with the number sent to the exchange. The dialled number is counted by C3, this counter counts user dialled pulses via the circuit in fig. 12; the output being transferred to the register as described earlier. When Autodialling is in progress pulses are counted directly from the dial pulse generator; in this case the register is disconnected from the counter. When the store is not addressed the outputs $S_A$-$S_D$ are all '0'. The register outputs $R_A$-$R_D$ are also '0' if Pulse out register is not selected. Thus the outputs of gates 20, 21, 22, and 23 are all high. When one of the pulsing out controls is operated the first digit appears in binary form at the inputs to these gates and in an inverted form at the outputs. A comparison is made with the contents of the counter C 3 (increasing as digits are being pulsed out), when the two are identical the output of gate 15 goes low and gate 38 high, indicating Parity (P). It will be noted that gate 14 output indicates whether there is any data presented for dialling, i.e. N is high if any of the inputs of the four NOR gates is high.

Fig. 15 details the circuit used to set the main control bistable J-K 1. It will be seen that when RECORD is selected 1 will be set if [0] is high, this indicates that the pulse train making up a digit has ended (I.D.P.). Setting also occurs if data is present and the control lock is free ('1'), or if there is Parity and Pr or Pw are selected. J-K 1 is shown in fig. 16. It will be seen that when it is set one lms clock pulse is switched by gates 28 and 32. If Pw='1' this shifts the contents of the register one place via gates 31 and 63, this pulse is also counted by C 4. As the setting condition is unchanged another three pulses will be gated, shifting the register contents four places in all. After four pulses the output of the counter, $SC_c$

goes high resetting J-K 1 via gate 19. The purpose of the setting condition applied to gate 45 is to shift data transferred to the register from counter C 3 during the I.D.P. between recorded digits. The gate 46 condition is a machine generated one that ensures that the four working bits of the 5-bit register are always kept clear when no control is applied. If this was not done the data seen by the Parity circuit would be incorrect, it is also a principle of register operation that four bits are always kept clear, in this way the start and end of the register number can be identified. The condition at gate 47 causes new data to be advanced when parity is reached; it will be noted that this condition applies for both Pr and Pw, however if Pw is selected $\overline{Pw}$ is low in which case gate 31 prevents the contents of the register from being shifted. Gate 58 also applies a '1' to K 1, this causes the J-K to reset after only one clock pulse has been gated. The outputs of counter C 4 are used as the selection lines for the store selectors (see fig. 9), in this way the store is scanned column by column. When a 'B' sub-store is addressed the selector (as always) first selects column 1 but sees no data as it has not been energised. As the contents of counter C 3 are zero Parity is high and the selector is stepped one column. Columns 2 to 4 will also have no data so Parity is maintained and the selector is rapidly stepped to column 5 (about 8ms) this column is the first of the 'B' sub-store and data may be found here in which case the control bistable is no longer set as Parity has fallen. Note that the procedure is similar for 'A' sub-stores, here the last four columns are skipped over at speed. Also note that if the 'A' and 'B' sub-stores are addressed simultaneously they will be read as an eight-digit store. When J-K 1 has reset and data is present (indicated by N high) the dial pulse generator control bistables, J-K 3 and 2 are set via gates 54 and 52 pulsing then starts as described earlier. At the end of pulsing, i.e. when Parity is high, new data is entered and the counter cleared, this is done during the I.D.P. so data is ready when the I.D.P. is complete, at which time pulsing begins again.

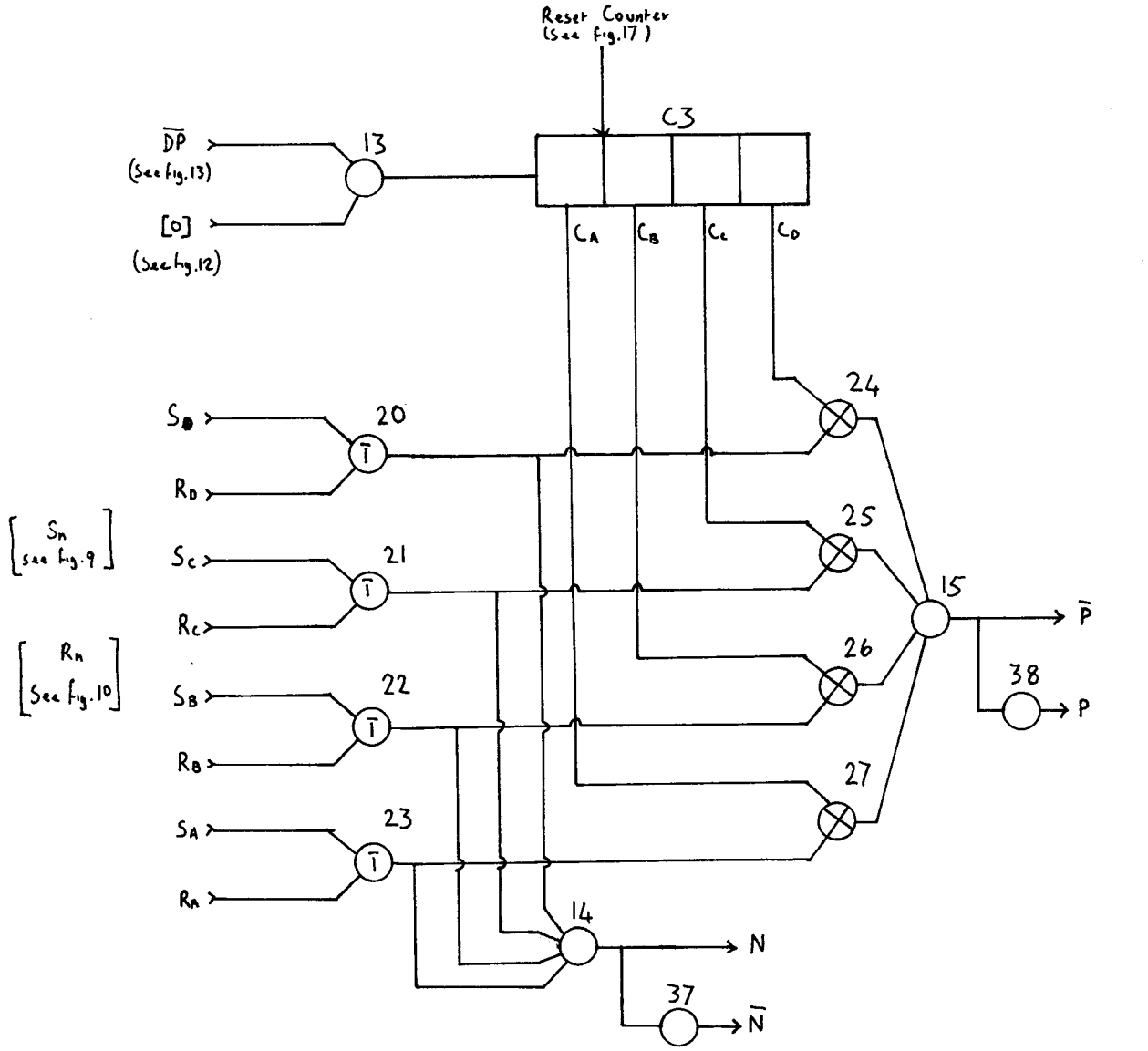



Fig. 14 Main Counter and Parity Circuit

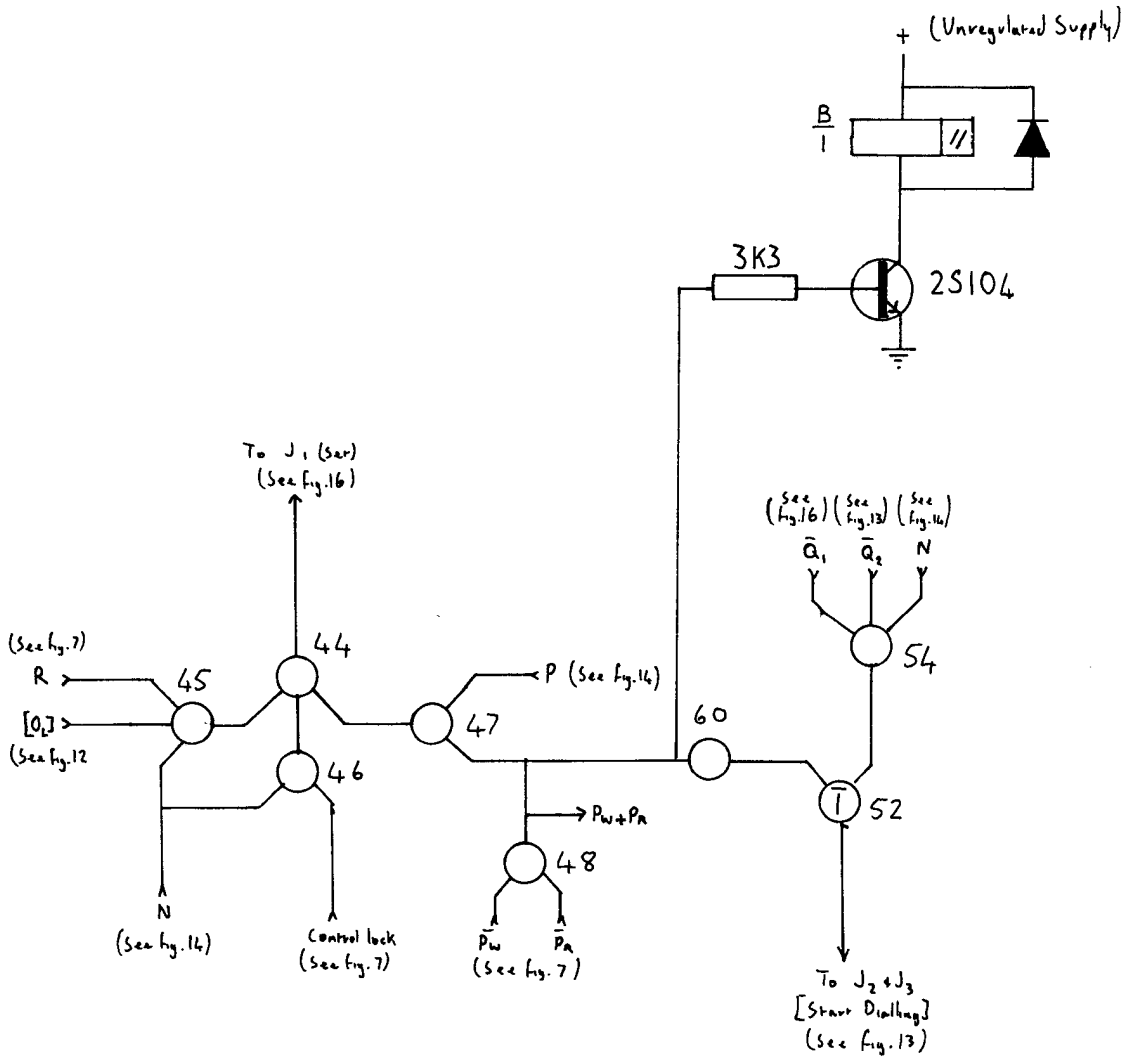



Fig. 15 Setting Circuit for Control Bistables

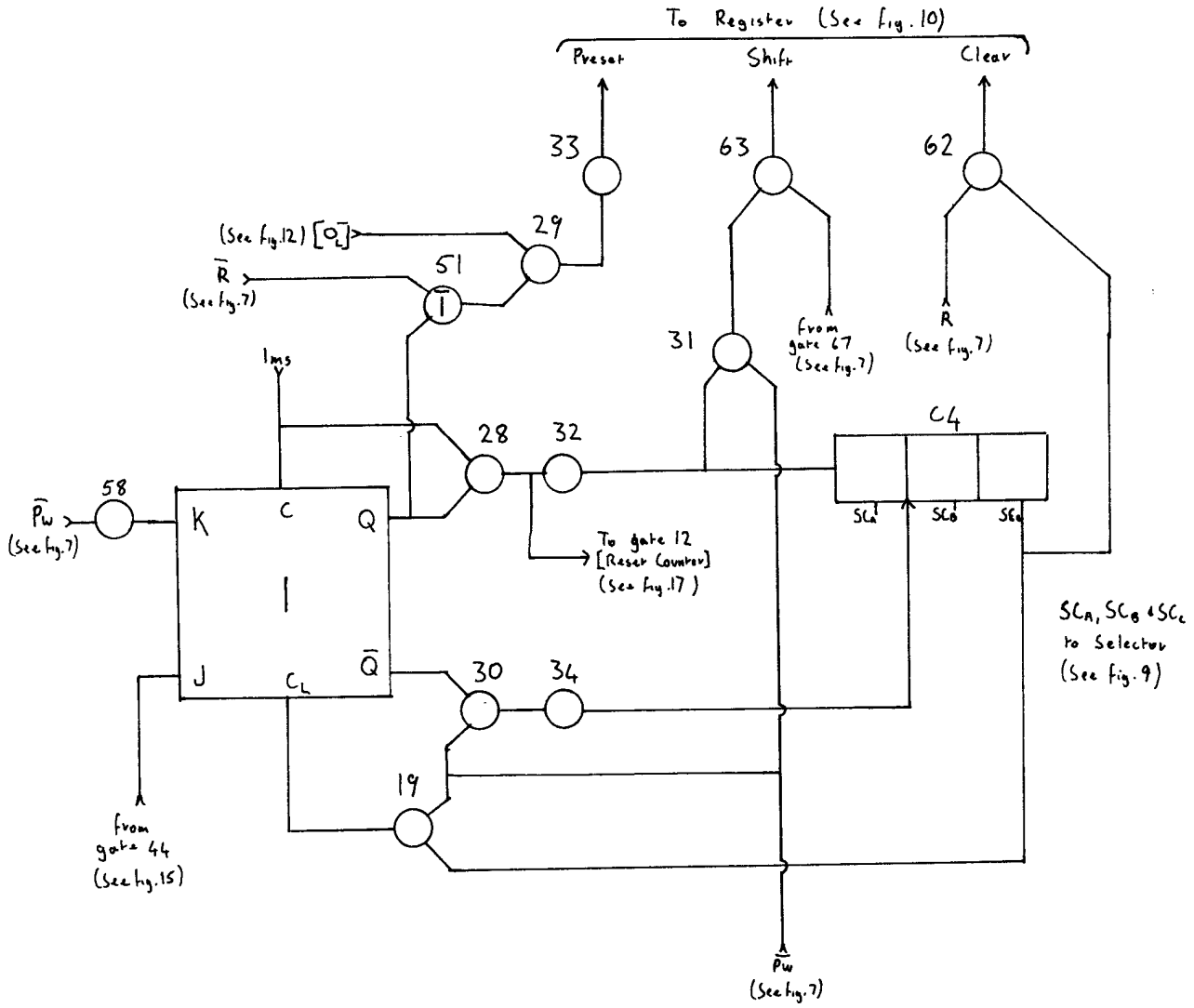



Fig. 16 Control Bistable J-K 1

Mention has been made of resetting the main counter C 3 this is carried out by gate 12, shown in fig. 17. This gate will reset the counter when no control is applied (control lock high) or if the output of gate 28 goes low it will be seen from fig. 16 that this will occur on the leading edge of the first shift pulse, when new data is being brought in.

When the timing of telephone dial pulses was described it was said that gate 2 caused resetting of the timing chain whenever the detector output changed, this is shown to occur via gate 16. When Autodialling is in progress the timing chain is not needed for pulse timing but a 32ms clock is required by the dial pulse generator. To ensure that this starts at the correct time the chain is reset when Pw or Pr are selected, via gates 18 and 16. When pulsing out is to begin $\overline{Q_2}$ goes low and this allows timing to start in phase with the start of pulsing out. If this were not done the first dial pulse would be of variable length.

There are three types of operation that can be initiated by the manual control; 1) Record 2) Pulse out Register and 3) Pulse out Store. When any of these operations have been started all other controls are locked out. After the operation has been performed this lock must be released and control returned to the user. A high input changing to a low input at gate 50 provides this release. The Record mode is cancelled when there is no number in the register, (i.e. the last digit has been shifted out of the 5-bit register) and the handset has been replaced. Inputs [$I_L$] and $\overline{N}$ to gates 65 and 64 do this. If Pulse out Register has been selected and the last number in the register has just been autodialled, $Q_2$ will still be high as the I.D.P. is timing, new data will be shifted in and $\overline{Q_1}$ will go high, but as the last digit has been shifted out the new data is zero, therefore $\overline{N}$ is now high. Resetting therefore takes place via 55, 65 and 64. In the case of a store number the last digit is known because all outputs of C 4 are high, these are grouped by gate 43. Control can obviously be returned to the user when the last digit has been autodialled, i.e. Parity high and the control J-K 1 reset. This condition is determined by gates 70,43,41 & 49.

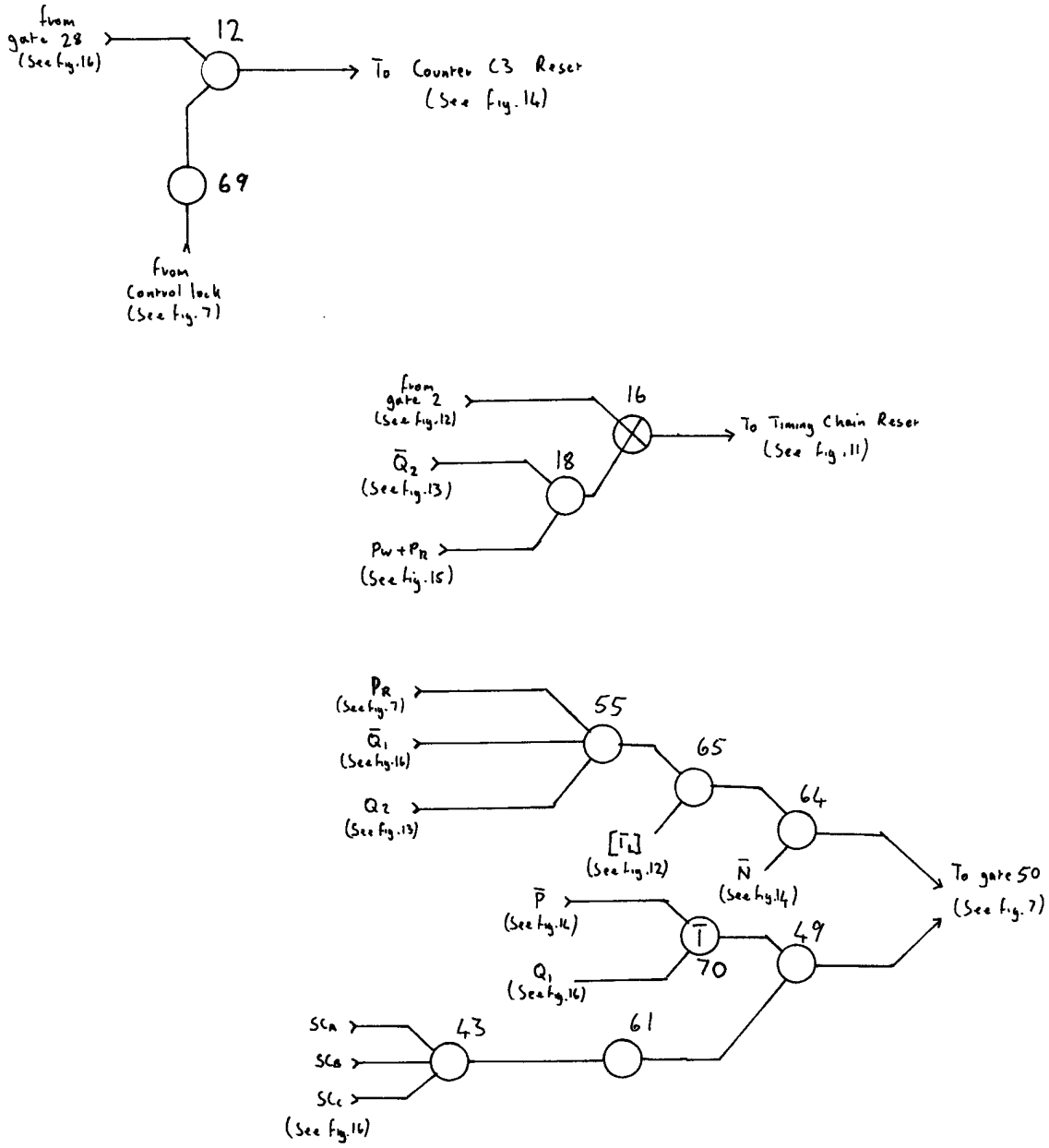



Fig. 17 Miscellaneous Reset Circuits

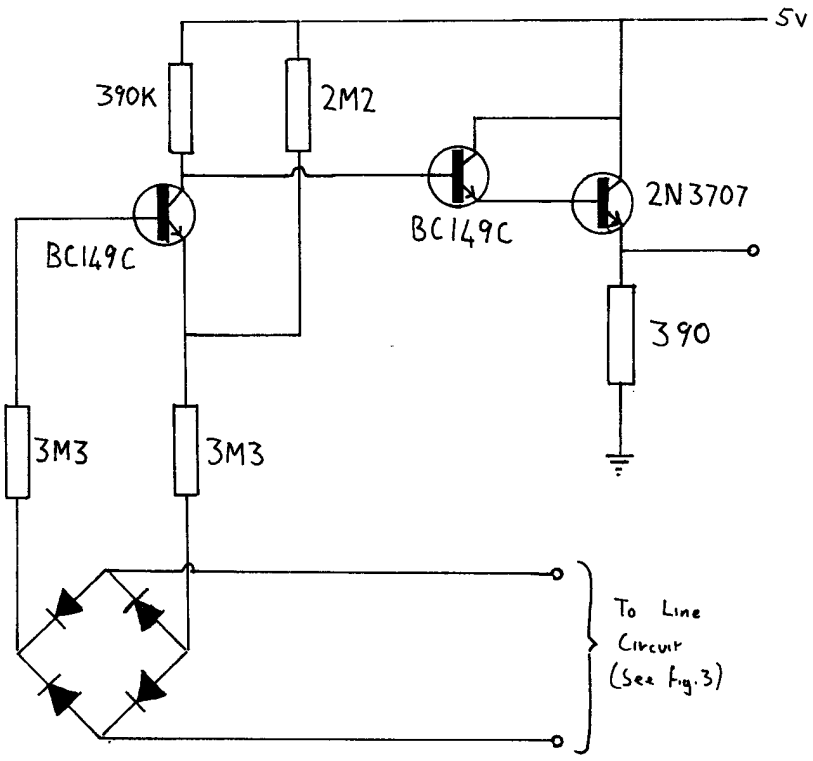



Fig. 18 Transistorised Detector